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FINLAND

Patents ADP number *(if you know it)* 05911995004

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Interface

This document describes a proposal for a standard low-pin count RF/BB interface for Bluetooth.

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1 Introduction

The purpose of this document is the specification of a standardized vendor and platform independent interface between the radio part (RF) and the baseband (BB) part of a Bluetooth (BT) system.

Important aspects of the Bluetooth system are described in co-pending UK patent application number GB9820859.8. The contents of these documents are hereby incorporated by reference, in particular, those parts relating to the implementation of the Bluetooth Low Power Radio Frequency System.

The benefit of a standardized interface is the interoperability of different RF and BB parts without HW changes. The low pin-count is particularly beneficial if the BB part is being integrated into another digital system e.g. a computer or phone chipset.

2 Interface Signals

The transfer of data and control information between the BB part and the RF part of a BT system is achieved using 2 three-wire interfaces (RFBus and Dbus) and an additional control signal SleepX.

The DBus is used to exchange general control data. The RFBus is used to transfer the transmitted and received data. In addition, time critical tasks during RX and TX are also performed via this bus.

Signal	Name	Direction	Function
1	RFBus1	bidirectional	RFBus
2	RFBus2	bidirectional	RFBus
3	BBClk	RF -> BB	RFBus (13 MHz)
4	DbusDa	Bidirectional	Dbus data
5	DbusClk	BB -> RF	Dbus clock
6	DbusEnX	BB -> RF	Dbus enable
7	VIO		Supply of the interfaces, 1.8V
8	SleepX	BB -> RF	

VIO supplies the voltage which the interfaces (RFBus, DBus SleepX) will use to define the logic levels. In this way, the interface can be run at a range of voltages to suit the particular application. At least a range of 1.8V+-10% need to be supported for VIO.

The VIO line is also used to supply the control circuitry to ensure that the system is controllable in power down mode.

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SleepX is a control signal from the BB part to the RF part. If SleepX==LOW, the RF part is in low power mode. Additionally, the internal control logic is forced into the "Control Mode" (see below) and thus performs a similar functionality as a usual reset signal. There is no activity permitted on the RFBus and the DBus if SleepX==LOW and the BBClk is switched off.

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2.1.1 RFBUS

The serial RFBus consists of 3 lines, that is BBClk, RFBus1 and RFBus2.
The BBClk is a 13 MHz clock generated in the RF part. It is used for synchronizing the data transferred via the RFBus. If applicable, it also might be used for clocking the logic of the baseband part.
Dependent on the mode of the RFBus, different functionality and direction of the signals RFBus1 and RFBus2 are specified.

Mode	Modes description	Functionality of the RFBUS1	Functionality of the RFBUS2	Direction of RFBUS1	Direction of RFBUS2
1	Control Mode	<CLKON>	0	BB -> RF	BB -> RF
2	Transmit Mode	<TXDATA>	<PAON>	BB -> RF	BB -> RF
3	Receive Mode	<RXDATA>	<DCTRACK>	RF -> BB	BB -> RF

The mode of the RFBus is controlled by the BB part. The state transitions are controlled via the DBus.

The CONTROL MODE is a neutral mode that is entered if neither RX nor TX mode applies. It is entered using the DBus or when SleepX==LOW. Thus SleepX can be considered as a reset signal as well. However, configuration registers in the RF part should not be reset using SleepX. They are programmed to their default states using the DBus. In Control mode, the signals RFBus1 and RFBus2 are driven by the BB part. In CONTROL MODE the 13 MHz clock (BBCLK) can be switched on by assigning RFBUS1==HIGH even if SleepX==LOW. Thus the clock is running if (SleepX==HIGH or (Mode=="Control Mode" and RFBUS1==HIGH)).

In TRANSMIT MODE the direction of RFBus1 and RFBus2 is from BB part to the RF part. RFBus1 is used to supply the digital transmit data <TXDATA> from the BB part to the RF part. Logic levels are used. The pulse shaping is done completely in the RF part and shall not depend on the value of VIO. Synchonization logic in the RF part shall ensure an exact symbol period of 1µs even if the data transferred on RFBus1=<TXDATA> exhibits substantial jitter. The line RFBus2 is used to control the timing of powering up the PA output stage of the RF part with RFBus2=<PAON>=HIGH.

In RECEIVE MODE the direction of RFBus1 is from RF part to the BB part and the direction of RFBus2 is from the BB part to the RF part. RFBus1 is used to supply sliced receive data at an oversampling ratio of 13 from the RF part to the BB part while using BBClk for synchronization. This is shown in the figure below.

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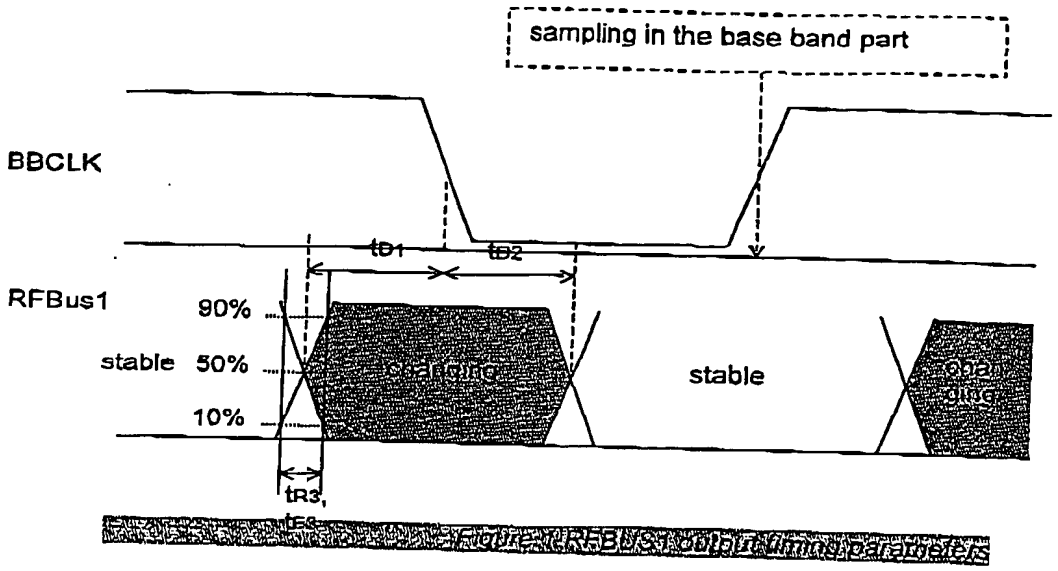

Figure: RFBus1 output timing parameters

The receive data <RXDATA> are provided as sliced data to the BB part. This implies that the DC estimation functionality (carrier offset compensation) resides in the RF part. By means of the signal RFBus2 the BB part can control the DC estimation into 2 different states. During <DCTRACK>=LOW a method for fast acquisition of a DC estimate shall be used (reception of start of a packet). During <DCTRACK>=HIGH, slower DC estimators may be used for reception of the remaining packet.

2.1.2 Serial IO Data Bus (DBus)

The serial IO Data Bus (DBus) is a basic Clock, Data and Enable serial interface. The following sections outline the addressing, data length, access allocations and detailed protocol of the DBus.

The DBus is not dedicated purely to the interface between the RF part and the BB part. In the event that the BB functionality is integrated into another host system, the DBus may also be used to communicate with other devices with a maximum of 32 data bits. Therefore the complete 8 address bits plus one R/W bit have to be verified before latching data to permit bus sharing with devices that are used concurrently to the Bluetooth RF part. In this event the data word lengths can vary.

The DBusEnX line should be used to block the DBusDa and DBusClk line activity at the boundary of the RF part. In the event the RF part will have a dedicated enable line, this would allow isolation of the RF part from disturbances caused by activity on these lines due to other devices using the same DBus.

The DBus shall be operational at DBus clock speeds of up to 20 MHz. Note that the DBus clock is sufficient to clock the interface in the RF part. The 13 MHz clock is not used in the implementation of the DBus interface and it is not permissible to assume timing relations between the 13MHz clock and the DBus clock.

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2.1.2.1 DBus Protocol

An access is always initiated by the DBus controlling device (e.g. the BT BB part). There are 3 device address bits and so a maximum of 8 devices can be addressed on the DBus. The device address of the BT RF part may either be programmable (using hard wired address pins) or fixed. If the BT RF part has a fixed address the address is 5 (101). Following the 3 device address bits there is a Read/Write bit which is then followed by 5 register address bits.

The preferred address allocation is:

Register Address Range	*Preferred Usage*
0-7	General programming, Mode control and RSSI reading (if applicable)
8-11	Control of optional 100mW PA (internal or external)
12-31	Reserved for future extensions

At the start of an access, the clock line (DBusClk) is reset to '0' and the Enable line (DBusEnX) is taken LOW half a clock cycle before the first positive clock edge to allow clean clock gating. At the first rising DBusClk edge the MSB of the address will be clocked into the RF part via the Data line (DBusDa).

The read and write access is arranged such that the addressed device will either read data or write data upon the rising edge of each clock pulse. This read and write protocol is described below. The Bluetooth RF part shall preferably be using 16 data bits after the address although the DBus protocol supports different lengths of the data words.

2.1.2.2 Dbus Write Access to the BT RF part

The controlling device will change the state of the data at the falling edge of each clock pulse. Following the 8 address bits, data bits are sent with the same timing as the address bits. Following the last data bit, the enable line is taken HIGH which indicates the arrival of the final data bit. The clock line then pulses one more pulse and is then held at '0' for a minimum of one cycle before a new access is started. The enable is therefore held HIGH for a minimum of two cycles.

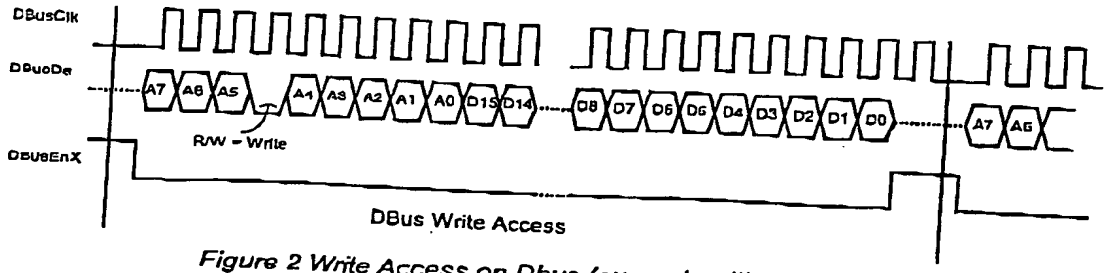

Figure 2 Write Access on Dbus (example with 16 bits of data)

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2.1.2.3 Read Access from the BT RF part

During a read access the addressed device generates data on the DBus to be read by the controlling device. This time, following the 8 address bits there is a turn around bit which lasts for half a clock cycle and has the effect of realigning the DBus timing such that now the addressed device will load bits onto the DBus upon the rising edge of the DBusClk. The bits are therefore read upon falling edges. Following the last address bit, the DBusClk is again disabled for at least one clock cycle before the next access.

As with the write access, the data word length for the read access is not fixed. The preferred value is 16 data bits. The controlling side of the interface determines the number of data bits by the use of the enable line. Thus, the data word length must be fixed for a certain address.

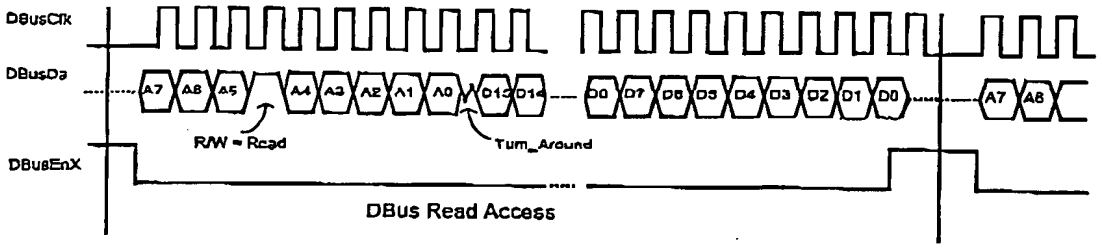

Figure 3 Read Access on Dbus (example with 16 bits of data)

2.1.2.4 DBus usage

All configuration data is send via the DBus as well as control words to switch between operational modes.

If data need to be read from the RF part (e.g. for RSSI measurements, etc.) the data is read digitally via the DBus rather than adding specific analog signals to the Interface.

During power down (SleepX=LOW) the DBus shall not be used to ensure very low current consumption from VIO.

3 List of Acronyms and Abbreviations

BB	Base Band
RF	Radio Frequency
RX	Receive
TX	Transmit

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1. The Current Situation

For control and data exchange between the baseband- and the RF-chip of e.g. a cellular phone, usually many signals for a control- and a data-interface are required. The needed amount of pins for both interfaces prevents to decrease the size of the chips as well as the board size. The power consumption may also be affected due to many toggling pins.

Especially for the low-cost, small-size and low-power Bluetooth system a RF-baseband interface with many lines is disadvantageous.

2. The new Solution

The proposed solution consists of only 7 interface lines. That is a 3-wire control interface, interacting with a 3-wire data interface together with a single Sleep-State control signal. The basic idea is to combine the generally usable control interface with the dedicated and exactly timed data interface in a way that the later can be used for multiple purposes during different states of the system.

The features of these interfaces are sketched below.

Table 1: Summary of the Interface Signals

Signal	Name	Direction	Function
1	DBusDa	bidirectional	Control Interface: data
2	DBusClk	BB -> RF	Control Interface: clock
3	DBusEnX	BB -> RF	Control Interface: enable
4	RFBus1	bidirectional	Data Interface: line 1
5	RFBus2	BB -> RF	Data Interface: line 2
6	BBCLK	RF -> BB	Data Interface: clock (e.g. 13 MHz)
7	SleepX	BB -> RF	Sleep-Mode control & reset

With the serial **3-wire control interface** the baseband chip is able to write / read the control block:

- This bus can be shared by up to 8 devices by distinguishing them by individual device addresses. See |1|.
- Set the RF-chip to one of its possible operating modes like RX, TX, RSSI measurement etc.
- Set the parameters of the control block like the synthesizer frequency
- Control test features for device test and for alignment procedures
- Read measured information like the signal strength at the input (RSSI)

The timing of this information is not critical. It is usually related to whole RX/TX-slots only. E.g. the synthesizer frequency is programmed at some time before the slot starts. Thus the real-time requirement is not as tight as that of the data-interface described below.

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The **3-wire data interface** is a dedicated bus for transferring time critical data between the baseband- and the RF-chip in both directions. The needed signals are:

- BBCLK: A synchronization clock for all signals on the data interface. It is generated by the RF-chip. (E.g. 13 MHz for a symbol rate of 1Mbaud @13 fold oversampling). It can also be used as the main clock source for the baseband chip.
- RFBus1: Bidirectional signal between baseband- and RF-chip; usage defined by the respective operating mode.
- RFBus2: Unidirectional signal from baseband- to RF-chip; usage defined by the respective operating mode.

The basic idea is not restricted to 2 data pins It can also be extended to a data interface with more pins if e.g. the data rate is too high for two pins.

Further with a **Sleep-State control signal** "SleepX" the baseband chip is directly able to control the reference oscillator, the power regulators and the default mode of the RF-chip as described later

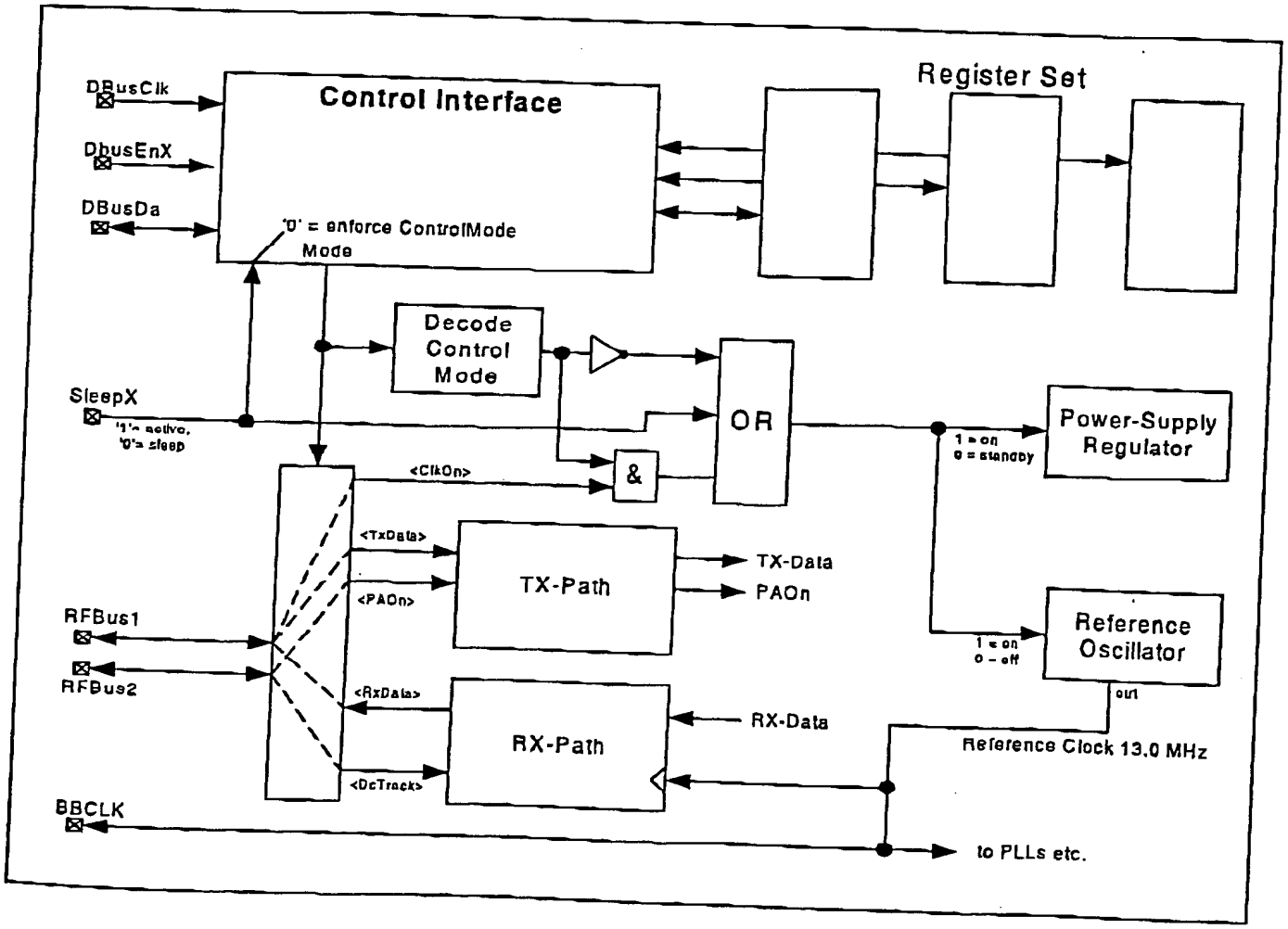

Figure 1: Structure of the Proposed RF-BB-Interface

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Essentially there are three operating modes of the RF-chip. Their number may be expanded if needed.

1. Control Mode
2. Transmit Mode (TX)
3. Receive Mode (RX)

2.1 System Startup

By using SleepX not only for controlling the Sleep-State but also as asynchronous reset for a few essential blocks, a dedicated reset pin can be avoided. It cannot be used as general reset e.g. for the configuration registers since it is repetitively activated. If SleepX = '0' (= sleep-state), the operating mode is asynchronously forced to "Control-Mode". In this mode neither transmission nor reception is active. At system reset, the BB-ASIC forces SleepX to '0' as long as its own reset is active.

Then it sets SleepX = '1' indicating an active system. Thus the crystal oscillator as well as the regulator is on. However during the short reset period, mentioned before, it must be assured that the oscillator and the main regulator is already on in order to supply the BB-ASIC. This is accomplished by using RFBus1 for a third purpose: If during "Control-Mode" RFBus1 = '1, the crystal oscillator as well as the regulator is forced on. The BB-ASIC must only assure this as the reset state of the corresponding pin.

After booting, the whole system is under control of the BB-ASIC and this pin can be released to its normal functionality. When entering the sleep-state (applying SleepX = '0') the BB-ASIC however must assure that the RFBus1 pin is set to '0' before. The details of this circuit can be found in Table 2.

SleepX = '0' may also be used for resetting the logic within the Rx and TX path. The register-set however should not be reset in order to avoid that it must be loaded again after each sleep-cycle. After booting the system, these registers are well defined. It must only be assured, that their contents don't influence the system during "Control-Mode".

Table 2 shows how the operating mode influences the function of the data-interface pins.

Table 2: Operating Modes and their Influence on the Data Interface

Mode Name	Functionality of RFBUS1	Functionality of RFBUS2	Direction of RFBUS1	Direction of RFBUS2
Control Mode	<CLKON>	0	BB → RF	BB → RF
Transmit Mode	<TXDATA>	<PAON>	BB → RF	BB → RF
Receive Mode	<RXDATA>	<DCTRACK>	BB ← RF	BB → RF

2.2 The Control Mode

The enforced mode during sleep-mode of the system (SleepX = '0') is the control-mode of the RF-chip. Here the signal **RFBus1** is used by the baseband chip for controlling the reference oscillator and the power regulators on the RF-chip. The functional signal is then "CLKON".

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When going to sleep-mode the baseband chip switches off the 13 MHz reference oscillator in order to save power. Further it is able to switch the power regulators to a low quiescent current mode because a sleeping system needs much less power compared to TX or RX.

In the control-mode the **RFBus2** signal is not needed. Therefore the baseband chip fixes the line to '0'.

2.3 The Transmit Mode

After having setup the RF-chip properly during control-mode via the 3-wire control interface (e.g. setting the TX frequency of the synthesizer), a control command sets the mode to TX-Mode.

Then the functionality of the data interface changes. Now the **RFBus1** signal is used for the serial TX-data coming from the baseband chip (functional signal name: "TXDATA").

The **RFBus2** signal is now used for precisely switching on/off the power amplifier of the RF-chip at the time determined by the burst-generator of the baseband chip. The functional signal name now is "PAON".

A synchronization logic on the RF-chip, operating with the low-jitter local reference clock BBCLK can be used to ensure an exact symbol period of the transmitted signal even if the TX-raw-data from the baseband chip exhibits substantial jitter.

2.4 The Receive Mode

During the gap between the TX-burst and Rx-burst the baseband chip reconfigures the RF-chip (e.g. switch the synthesizer to the Rx frequency) and switches to Rx-mode. Here the RF-chip will place the sliced and 13 fold oversampled raw data on the **RFBus1** line for further processing within the baseband chip. BBCLK will be the corresponding oversampling clock.

At the same time the baseband chip will use the **RFBus2** line to aid the DC-estimator within the demodulator (switch between fast acquisition and slow tracking).

3. The Control-Bus Protocol

The 3-wire control bus is a clock, data and enable serial bidirectional interface. The description of the detailed protocol can be found in [1]. It is also possible to use another type of protocol like I^2C ©, as long as the speed is high enough.

Figure 1 illustrares RFBus1 output timing parameters;
Figure 2 illustrares Write Access on Dbus;
Figure 3 illustrates Read Acccss on Dbus;
Figure 4 illustrates the RF side of the RF-BB interface;
Figure 5 illustrates the BB side of the RF-BB interface;
Figure 6 illustrates how the Dbus may control devices inaddition ro the LPRF RF chip;
Figure 7 is a schematic illustration of a LPRF transceiver illustrating the functionality of RFBus;
Figure 8a illustrates how RFBus is configured and how the RF chip responds in the control mode;
Figure 8b illustrates how RFBus is configured and how the RF chip responds in the transmit mode;
Figure 8c illustrates how RFBus is configured and how the RF chip responds in the receive modc;
Figure 9 is a flow chart illustrating the control mode.

The Dbus (DbusDa, DbusEnX and DbusClk) is used to control the LPRF RF chip and other devices as illustrated in Figure 6. The Dbus writes data to and reads data from registers in the LPRF RF chip. The registers writen to may include a register which controls the frequency at which the RF chip transmits or receives and may a register which controls the power at which the RF chip transmits and registers which identify wgether the RF chip is in the control, transmit or receive mode. The registers read from may include a register containing RSSI information. Thus the Dbus may control the operation of the LPRF RF chip, for example, controlling the transition from receiving to transmitting. However, the Dbus is not efficient at controlling time critical tasks in the RF chip which need to be carried out immediately.

The Burst Mode Controller provides to a serial control interface data, address information, information identifying whether a write or read operation is required and a trigger signal provided by a timing control unit controls the timing of the operation. The serial control interface converts the supplied signal to a Dbus signal. The microcontroller

may also provide data to the RF chip via the serial control interface. This is advantageous on boot-up. The microcontroller controls whether the serial control interface takes data from the microcontroller or the burst mode controller.

The burst mode controller as controls the contents of RFBus. RFBus 1 is a bidirectional. In the transmit mode the RFBus 1 provides data to the RF chip for transmission. In the receive mode RFBus 2 receives data from the RF chip.

RFBus 2 is used to control time critical tasks in the RF chip. It is fast at transmitting control signals from the BB engine to the RF chip. In the transmit mode, RFBus2 is used to control the timing of the Power Amplifier. In the receive mode RFBus 2 is used to control the timing of the DC estimator cganging from a fast data acquisition mode to a slower data acquisition mode.

The RFBus is used for different purposes during different states, as illustrated in Figures 8a, 8b, and 8c. How RFBus controls the transceiver of the RF chip is illustrated in Figure 7.

The operation of a LPRF device is described in detail in UK Patent Application No 9820859.8 . the contents of which are hereby incorporated by refernce. In particular Figure 3 shows LPRF RF components of a transceiver (Tx, Rx and Frequency control), connected to baseband components (the remaining elements in the Figure).

The present invention includes any novel faeature or combination of features disclosed herein either explicitly or implicitly or any generalisation thereof.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made to the foregoing description without departing from the scope of the invention.

Claims

1. A device having an interface for controlling an RF transceiver, the interface having: a plurality of connectors for providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode: at least first and second connectors wherein in a first mode, one of said first and second connectors supplies data to the transceiver and the other is operable to provide a first control signal to the transceiver and wherein, in the second mode, one of said first and second connectors receives data from said RF module and the other is operable to provide a second different control signal to the transceiver.

2. A device as claimed in clim 1 wherein the first and second control signals are time critical control signals.

3. A dveice as claimed in any preceding claim wherein time critical control signals are not provoded via said plurality of connectors.

4. A device as claimed in any preceding claim wherein the first mode is a transmit mode for the transceiver.

5. A device as claimed in any preceding claim wherein the second mode is a receive mode of the transceiver.

6. A device as claimed in any preceding claim having a third connector (SleepX) for powering down components of the transceiver.

7. A device as claimed in any preceding claim wherein the first connector is bi-directional and supplies data in the first mode and receives data in the second mode.

8. A device as claimed in any preceding claim wherein the first control signal controls the power amplifier of the transmitter portion of the transceiver.

9. A device as claimed in any preceding claim wherein the second control signal controls dc estimation of the data received by the receiving portion of the transceiver.

10. A device as claimed in any preceding claim whercin thc plurality of connectors includes a connector for transferring data to and from the device, a connector for providing, an enable signal from the device and a connector for providing a clock signal from the device.

11. A device as claimed in any preceding claim further comprising a connector for receicing a clock signal from the transceiver.

12. A dcvicc as claimed in any preceding claim wherein the plurality of connectors are used o read from and write to registers in the transceivcr

13. A dcvicc as claimed in any preceding claim wherein the plurality of connectors is a serial interface having at least one connector via which data is transmitted in serially, siad data including a device addrtess, a bit indicating whether data is for writing or has been read, a local address and a variable data portion.

14. A device as claimed in claim 13 wherein the data portion may have a length varying between 1 and 32 bits.

15. A device as claimed in any preceding claim wherein the plurality of connectors are coupled to at least one other device.

16. Transceiver circuitry having an interface for connection to a device having baseband circuitry, the interfacc having:

a plurality of connectors for providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode;

at least first and second connectors wherein in a first mode, data is received at one of said first and second connectors and a first control signal is receivable at the other and wherein, in the second mode, data is provided at one of said first and second connectors for transfer to the device and a second different control signal is receivable at the other.

17 A method of interfacing a device having a baseband engine to a transceiver, the device having means for controlling whether the transceiver is in a transmitting mode or a receiving mode and first and second connectors, comprising the steps of:
controlling the transceiver to enter the transmitting mode;
providing data from the device to the transceiver via the first connector; and
controlling the power amplifier in the transceiver via the second connector

18 A method of interfacing a device having a baseband engine to a transceiver, the device having means for controlling whether the transceiver is in a transmitting mode or a receiving mode and first and second connectors, comprising the steps of:
controlling the transceiver to enter the receiving mode;
receiving data at the device from the transceiver via the first connector; and
controlling the dc estimation in the transceiver via the second connector.

19. An interface having connectors including a first connector for controlling time critical functions , said time critical function being dependent upon whether another connector receives or provides data.

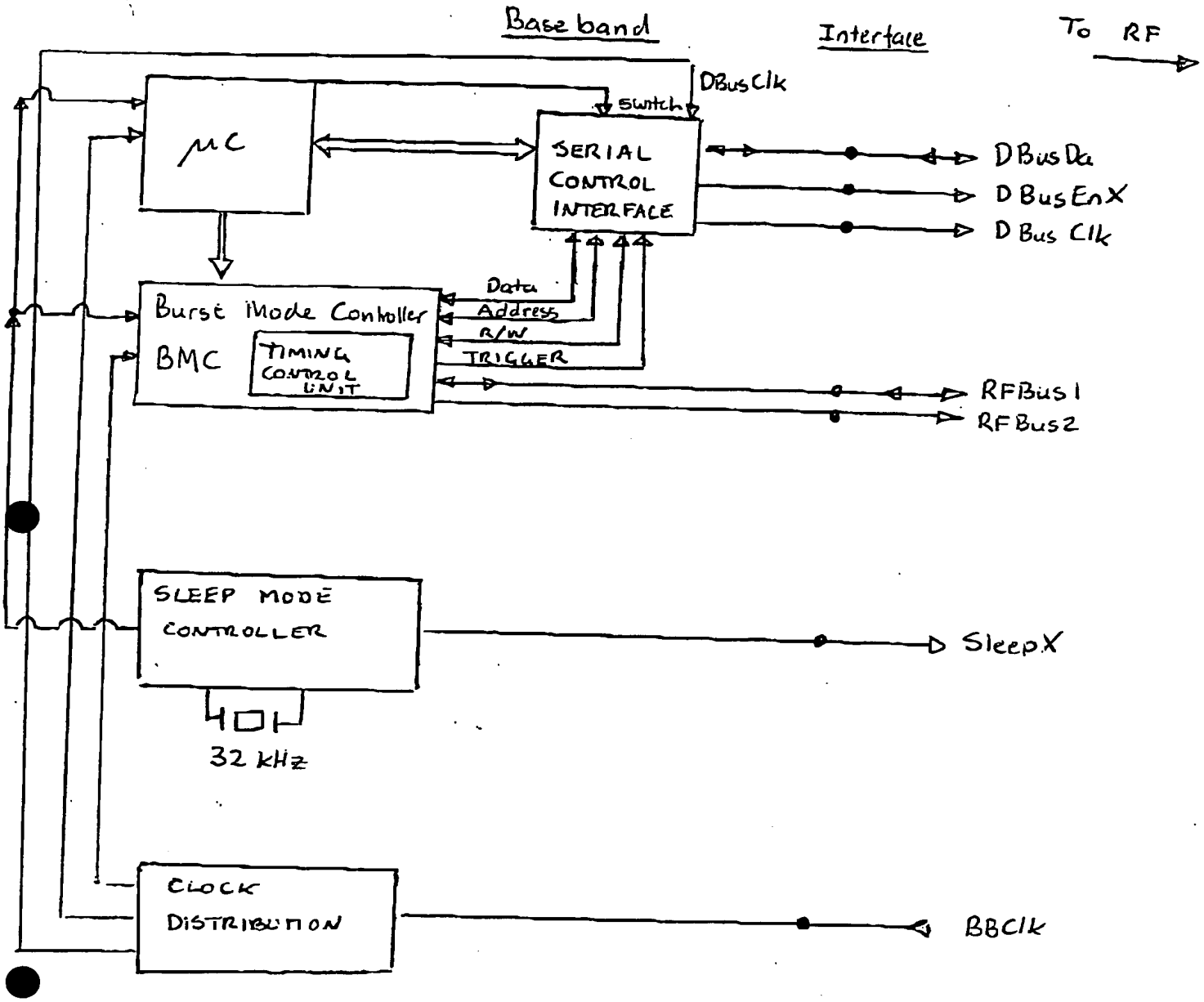

Base band
Interface
To RF
DBusClk
switch
µC
SERIAL CONTROL INTERFACE
DBusDa
DBusEnX
DBus Clk
Burst Mode Controller
BMC
TIMING CONTROL UNIT
Data
Address
R/W
TRIGGER
RFBus1
RFBus2
SLEEP MODE CONTROLLER
SleepX
32 kHz
CLOCK DISTRIBUTION
BBClk

Fig 5

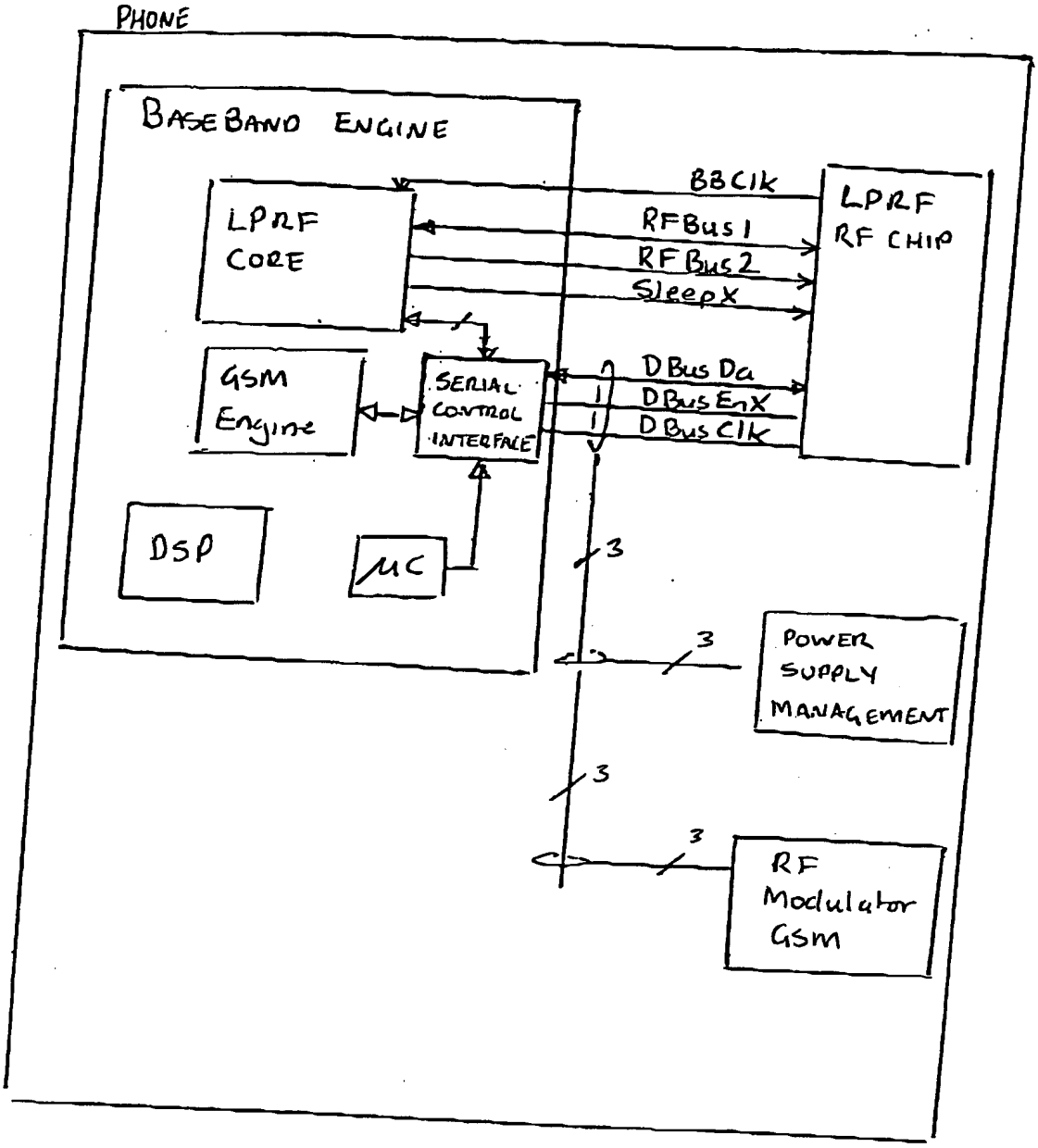
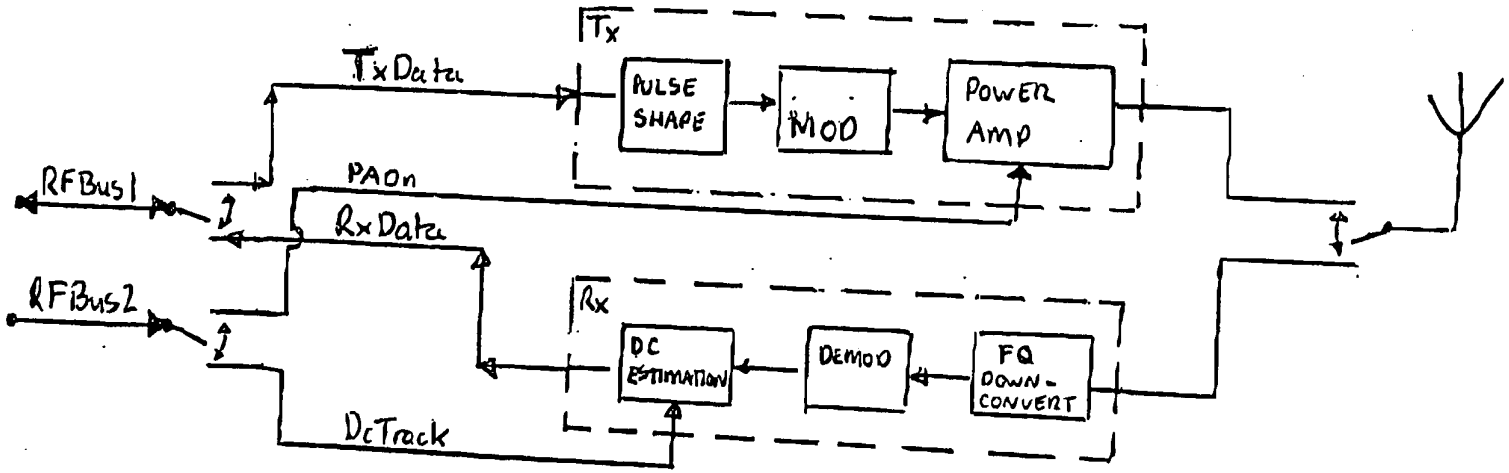

PHONE
BASEBAND ENGINE
LPRF CORE
BBClk
RFBus1
RFBus2
SleepX
LPRF RF CHIP
GSM Engine
SERIAL CONTROL INTERFACE
DBus Da
DBus EnX
DBus Clk
DSP
µC
3
3
POWER SUPPLY MANAGEMENT
3
3
RF Modulator GSM

Fig 6



In Tx Mode - switches UP

In Rx Mode - switches DOWN

Fig 7

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NTROL MODE OF RF TRANSCEIVER

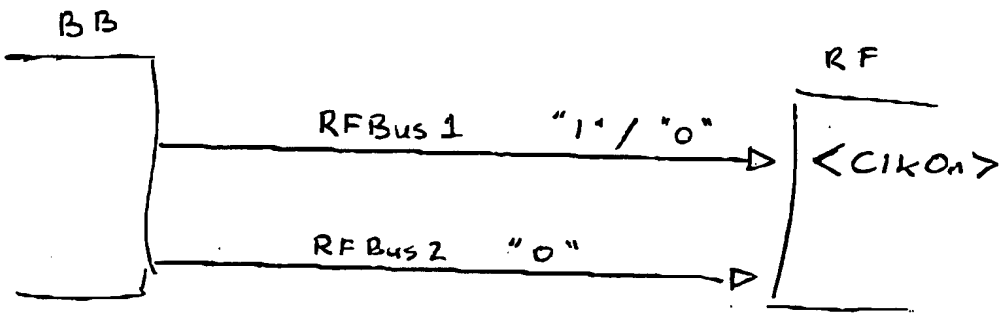

Fig 8a

TRANSMIT MODE OF RF TRANSCEIVER

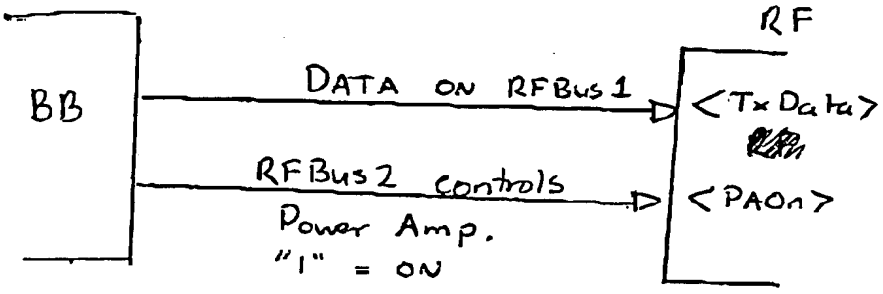

Fig 8b

RECEIVE MODE OF RF TRANSCEIVER

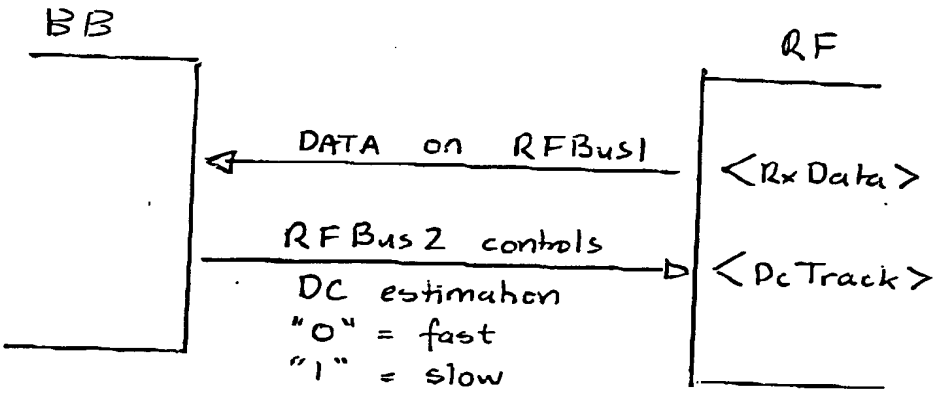

Fig 8c

CONTROL MODE

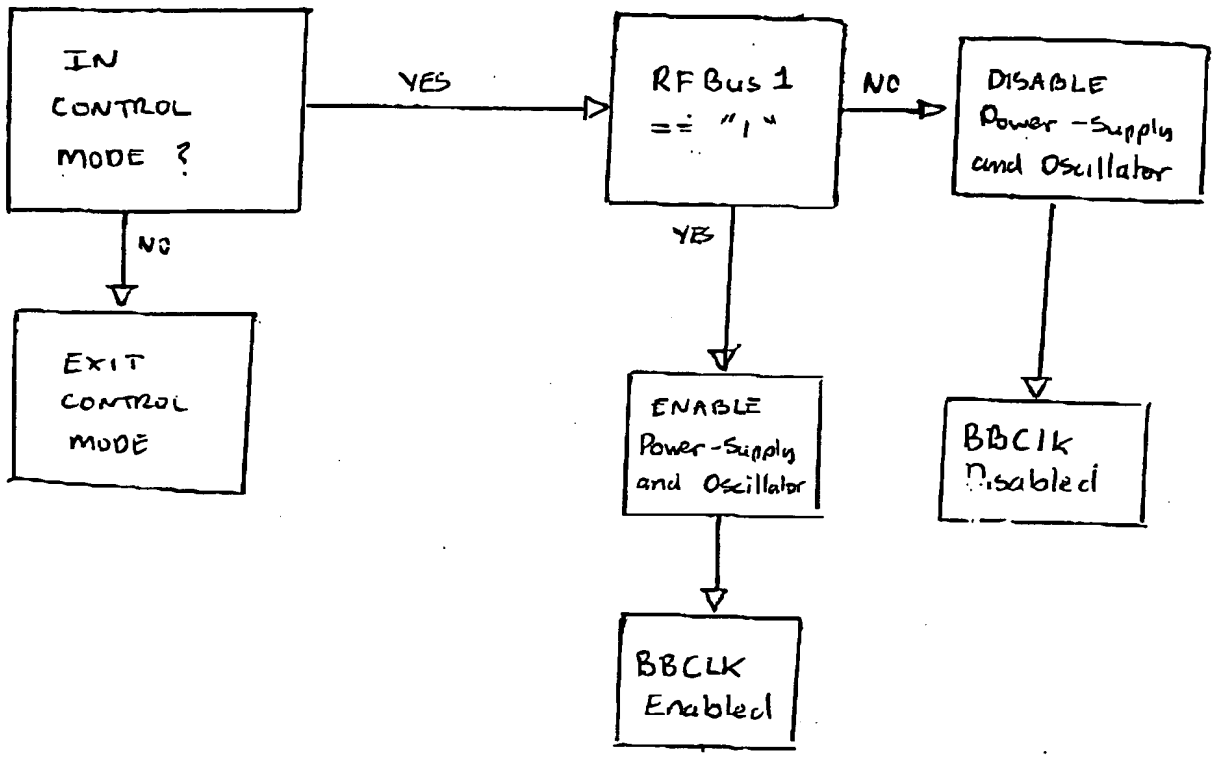

Fig 9.

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